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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/773,595 | 02/02/2001 | Atsushi Yoshikawa | 088941/0184 | 6240 |

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| EXAMINER | |
|---|---|
| DU, THUAN N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2116 | |

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/773,595 | YOSHIKAWA ET AL. | |
| | Examiner | Art Unit | |
| | Thuan N. Du | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment and Drawings (dated 8/16/04).

2. Claims 1-15 are presented for examination.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-8, 10-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitations "the delay time interval" (l. 2), "the output side of a specified gate" (l. 4), "the output side of said first gate" (l. 6), "said input signal" (l. 7-8) and "the number of gate stages" (l. 11-12). There is insufficient antecedent basis for these limitations in the claim. Furthermore, it is not clear whether "a first switching device" and " a second switching device" recite in line 9 are the same or different from switching devices recite in lines 5 and 7.

Claim 2 recites the limitations "the gate output load" (l. 3-4) and "the register value" (l. 5). There is insufficient antecedent basis for these limitations in the claim.

Claim 3 recites the limitations "the output value" (l. 3) and "the register value" (l. 5). There is insufficient antecedent basis for these limitations in the claim.

Claim 4 recites the limitation "the output signal" (l. 4). There is insufficient antecedent basis for this limitation in the claim.

Claim 5 is also rejected for incorporating the above deficiency by dependency.

Claim 6 recites the limitations "the output signal" (l. 3-4), "the output" (l. 6), "the non-operational mode" (l. 7), "the operational mode" (l. 10) and "the logical processing" (l.10). There is insufficient antecedent basis for these limitations in the claim. Furthermore, it is not clear whether "a reference clock" in line 3 is the same or different from reference clock recited in line 2, "a clock" in line 8 is the same or different from a clock recited in line 4.

Claim 7 recites the limitations "the duty ration" (l. 3), "the register value" (l. 5) and "the detected output" (l. 6). There is insufficient antecedent basis for these limitations in the claim.

Claim 8 recites the limitations "the register value" (l. 4) and "the detected output" (l. 5). There is insufficient antecedent basis for these limitations in the claim.

Claim 10 recites the limitations "the input terminals" (l. 5), "the input" (l. 6), "the output" (l. 6-7), "the outputs" (l. 7), "the exclusive AND" (l. 13) and "the output signals" (l. 13). There is insufficient antecedent basis for these limitations in the claim.

Claim 11 recites the limitation "the exclusive AND" in line 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the output signal" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "the output signal" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 14 recites the limitations "the output signal" (l. 4-5), "the output" (l. 7), "the non-operational mode" (l. 8), "the operational mode" (l. 11) and "the logical processing" (l.11). There is insufficient antecedent basis for these limitations in the claim. Furthermore, it is not clear whether "a reference clock" in line 4 is the same or different from reference clock recited in line 2, "a clock" in line 9 is the same or different from a clock recited in line 5.

Claim 15 recites the limitations "the output signal" (l. 4-5), "the output" (l. 7), "the non-operational mode" (l. 8), "the operational mode" (l. 11) and "the logical processing" (l.11). There is insufficient antecedent basis for these limitations in the claim. Furthermore, it is not clear whether "a reference clock" in line 4 is the same or different from reference clock recited in line 2, "a clock" in line 9 is the same or different from a clock recited in line 5.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al. [Goto] "CMOS Programmable Delay Vernier" – October 1994 – Hewlett-Packard Journal.

7. Regarding claim 1, Goto teaches a delay adjustment circuit comprising:

a first gate array for carrying out fine adjustment of the delay time interval that has each gate serially connected [Page 53, Fig. 4b, FE elements];

capacitance connected to the gate via a first switching device [Fig. 5];

a second gate array that is connected to the output side of said first gate array via a second switch device and carries out rough adjustment of delay time interval of said input signal [Page 53, Fig. 4b, CE elements incorporate with Multiplexer];

a control device that control first switching device [Fig. 5, Digital Control] as to adjust the delay time interval by adjusting the capacitance connected [p. 54, col. 1, "Delay Vernier Element Design"].

Goto does not explicitly teach the control device for controlling the second switch. One of ordinary skill in the art would have recognized that the multiplexer obviously receives a control signal for selecting the output signal.

8. Regarding claims 2 and 3, Goto teaches all the circuitries and elements are formed on an IC device [Figs. 1, 2].

9. Regarding claims 9-11, Goto teaches a clock generating circuit [ACCEL2] comprising:

a delay adjustment circuit [Page 53, Fig. 4] having a delay time interval that can be adjusted by internal capacitors [p. 54, col. 1, 2nd paragraph]; and

a logic circuit [Page 53, Fig. 4b; multiplexer] that outputs a clock having a desired frequency [FE out] by carrying out logic operations on one or more signals [p. 53, col. 2, last paragraph et seq.], these signals being the input signals that have been delayed a specified time interval by the delay circuit [Page 53, Fig. 4b; the signals inputted to the multiplexer].

Goto does not explicitly teach the delay time interval can be adjusted by internal register values, internal memory values and internal logic signal. One of ordinary skill in the art would have readily recognized that it would have been obvious to use these values or any other desired values as a trigger to turn on and off the internal capacitors.

10. Claims 4-6 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goto et al. [Goto] "CMOS Programmable Delay Vernier" – October 1994 – Hewlett-Packard Journal and applicant's admission of prior art [AAPA].

11. Regarding claims 4, 6 and 12-15, Goto teaches that the delay adjustment circuit into which a reference clock is input [p. 56, col. 1, last paragraph].

Goto does not explicitly teach the system including a logic circuit that outputs a clock having an operational frequency N times the reference clock.

AAPA teaches a clock generating circuit comprising a logic circuit that outputs a clock having an operational frequency N times the reference clock [application's specification, p. 1, lines 13-20].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Goto and AAPA because they both teach system for generating clock signal. AAPA teaching of generating a clock having an operational frequency N times the reference clock would increase the flexibility of the system by allowing the system receiving a low operational frequency reference clock and outputting a higher operational frequency clock depends on the need of the system.

12. Regarding claim 5, Goto teaches the system including flip flops [Fig. 3; p. 52, col. 1, last paragraph].

### *Allowable Subject Matter*

13. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and correcting all of the outstanding deficiency mentioned above.

### *Response to Arguments*

14. In the Remarks (dated 8/16/04), applicant argued that Fig. 4 of Goto is a graph which does not indicate the "FE." The Fig. 4 and/or Fig. 4b which examiner relied upon is on page 53, not the Fig. 4 on page 55 which belongs to the "Theoretical Approach to CMOS Inverter Jitter."

### *Conclusion*

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan N. Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday and Wednesday-Friday: 10:00 AM - 8:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
November 12, 2004